

AO3422

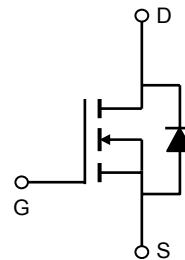
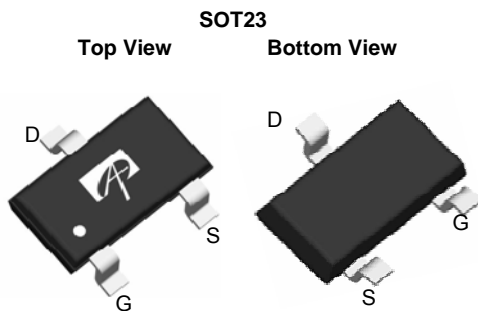
N-Channel Enhancement Mode Field Effect Transistor

General Description

The AO3422 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. It offers operation over a wide gate drive range from 2.5V to 12V. This device is suitable for use as a load switch.

Features

V_{DS} (V) = 55V
 I_D = 2.1A (V_{GS} = 4.5V)
 $R_{DS(ON)} < 160m\Omega$ (V_{GS} = 4.5V)
 $R_{DS(ON)} < 200m\Omega$ (V_{GS} = 2.5V)



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	55	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ^A	$T_A=25^\circ\text{C}$	2.1	A
		$T_A=70^\circ\text{C}$	
Pulsed Drain Current ^B	I_{DM}	10	
Power Dissipation	$T_A=25^\circ\text{C}$	1.25	W
		$T_A=70^\circ\text{C}$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	75	100	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Ambient ^A		Steady-State	115	150
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	48	60	$^\circ\text{C}/\text{W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =10mA, V _{GS} =0V	55			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =44V, V _{GS} =0V			1	μA
		T _J =55°C			5	
I _{GSS}	Gate-Source leakage current	V _{DS} =0V, V _{GS} =±12V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.6	1.3	2	V
I _{D(ON)}	On state drain current	V _{GS} =4.5V, V _{DS} =5V	10			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =4.5V, I _D =2.1A		125	160	mΩ
		T _J =125°C		175	210	
		V _{GS} =2.5V, I _D =1.5A		157	200	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =2.1A		11		S
V _{SD}	Diode Forward Voltage	I _S =1A		0.78	1	V
I _S	Maximum Body-Diode Continuous Current				1	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =25V, f=1MHz		214	300	pF
C _{oss}	Output Capacitance			31		pF
C _{rss}	Reverse Transfer Capacitance			12.6		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		1.3	3	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =27.5V, I _D =2.1A		2.6	3.3	nC
Q _{gs}	Gate Source Charge			0.6		nC
Q _{gd}	Gate Drain Charge			0.8		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =27.5V, R _L =12Ω, R _{GEN} =3Ω		2.3		ns
t _r	Turn-On Rise Time			2.4		ns
t _{D(off)}	Turn-Off DelayTime			16.5		ns
t _f	Turn-Off Fall Time			2		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =2.1A, dI/dt=100A/μs		20	30	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =2.1A, dI/dt=100A/μs		17		nC

A: The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t_{θJA} ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

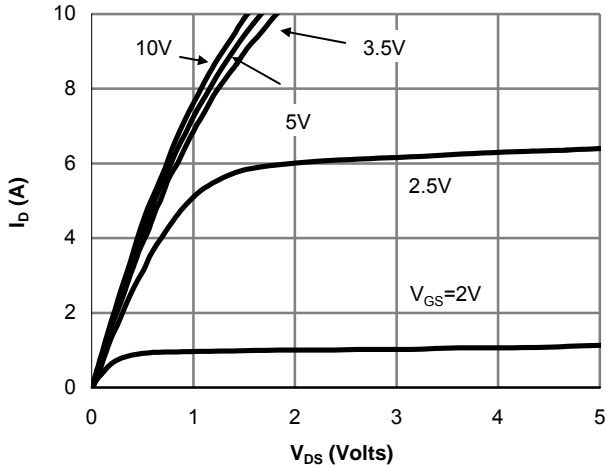


Fig 1: On-Region characteristics

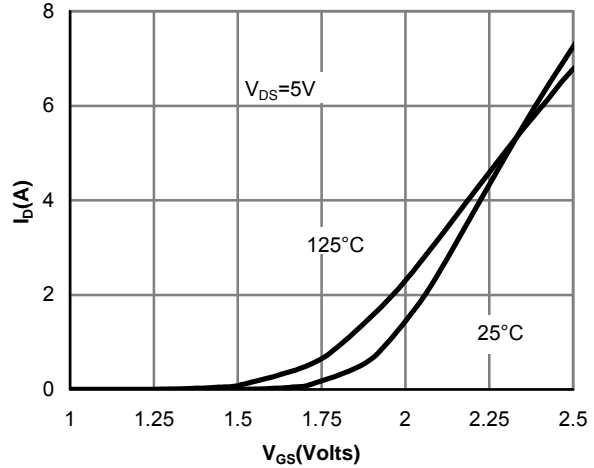


Figure 2: Transfer Characteristics

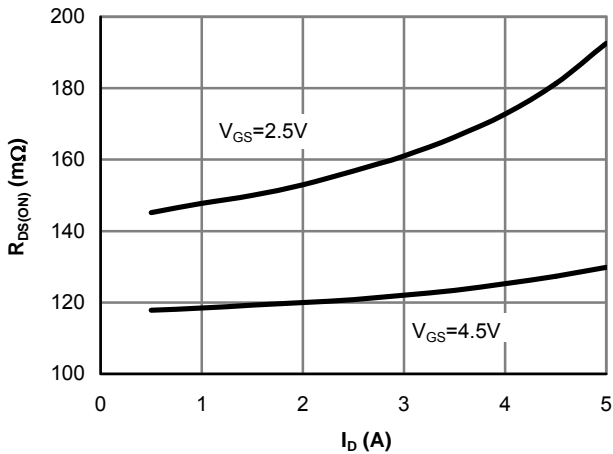


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

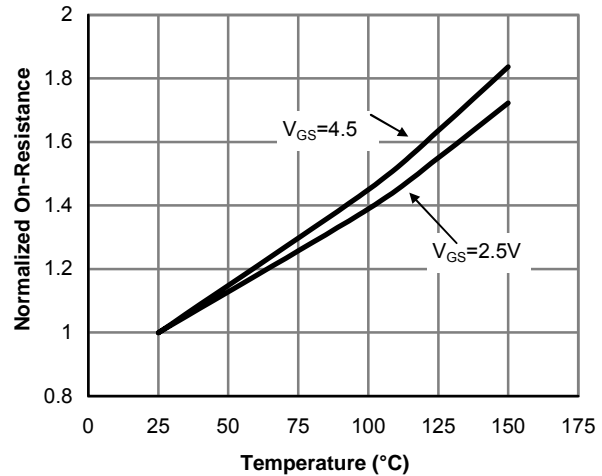


Figure 4: On-Resistance vs. Junction Temperature

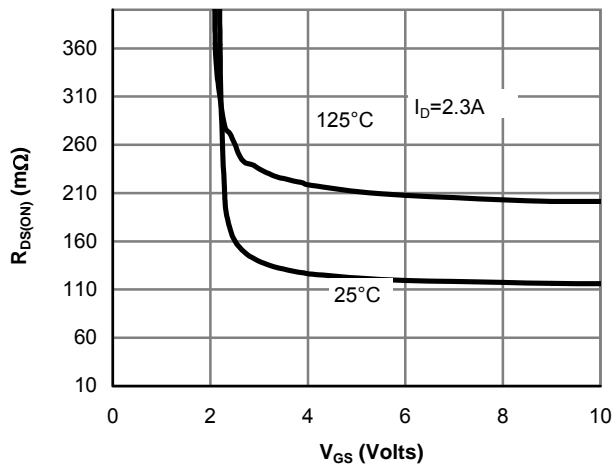


Figure 5: On-Resistance vs. Gate-Source Voltage

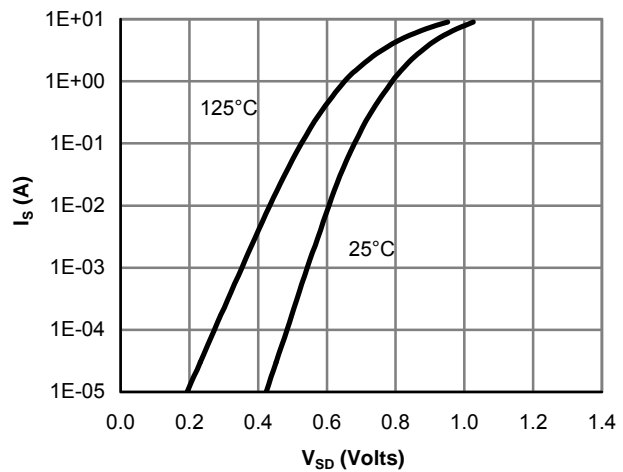


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

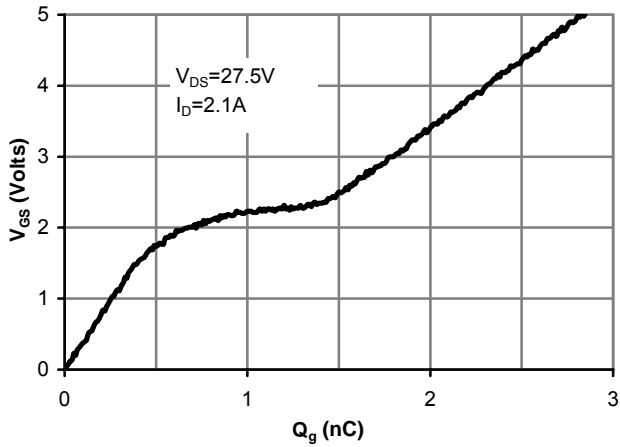


Figure 7: Gate-Charge Characteristics

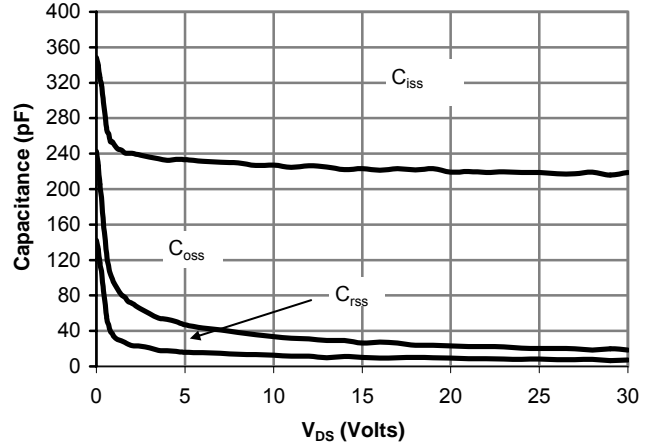


Figure 8: Capacitance Characteristics

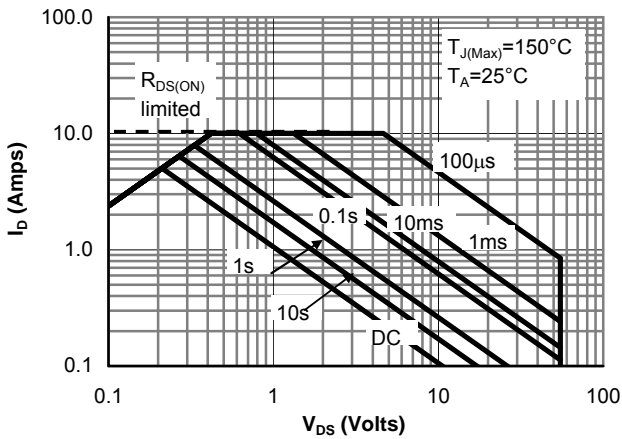


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

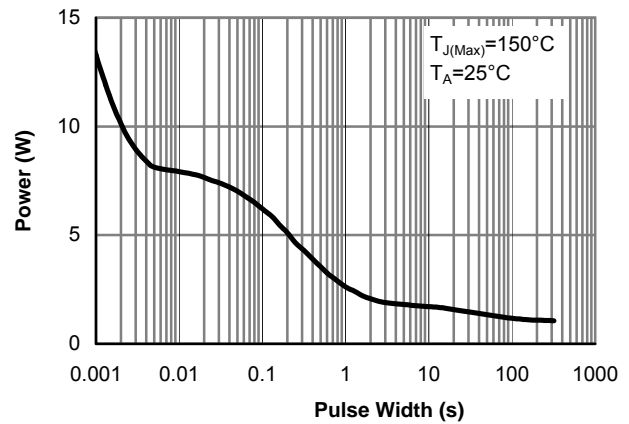


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

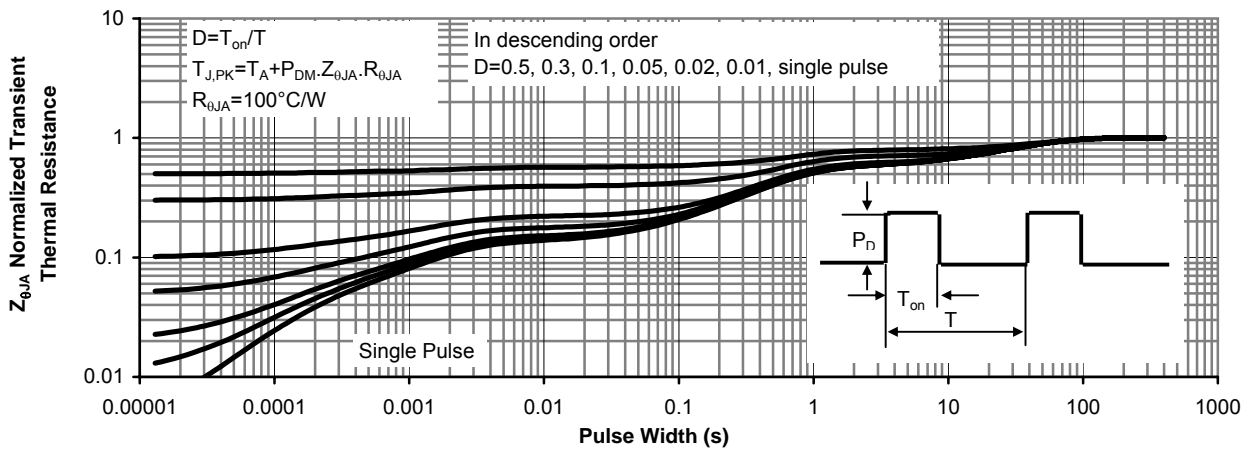
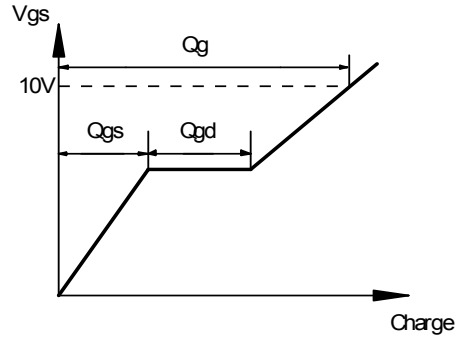
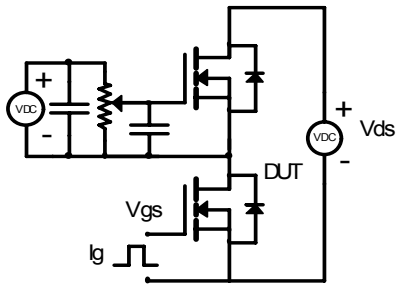
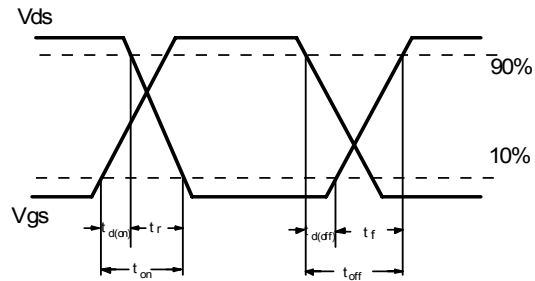
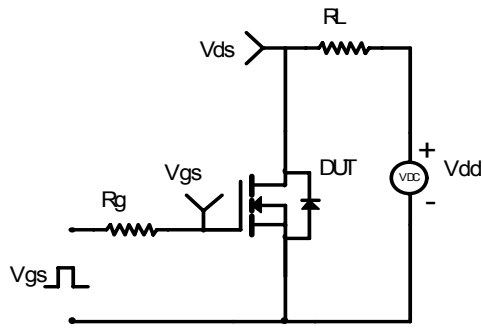


Figure 11: Normalized Maximum Transient Thermal Impedance

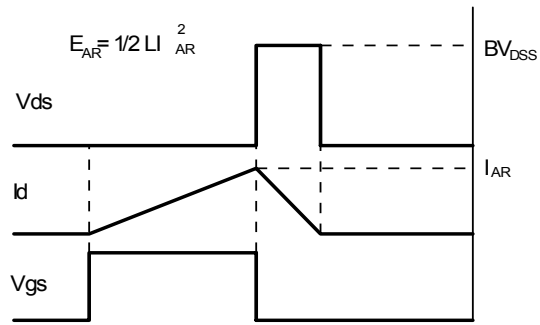
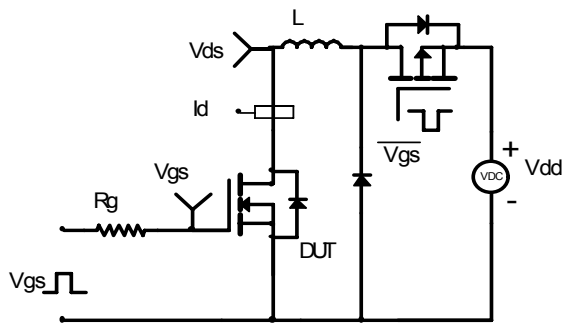
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

